ICECS 2012 TUTORIAL PROPOSAL

Title: Digital Delta-Sigma Modulators for DAC and Fractional-N Frequency Synthesis Applications

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Abstract

Delta-Sigma Modulation (DSM) is increasingly used in digital to analog converters and frequency synthesizers. Classical analysis of DSM makes assumptions about quantisation that promote linear ways of thinking. Many of the unexpected phenomena that degrade the performance of real systems are due to underlying nonlinear effects. The use of finite state machines adds a further level of complexity. This tutorial is in four parts. Part I addresses ideal Digital Delta-Sigma Modulator (DDSM), explains what signal processing assumptions are commonly made to understand its operation, and presents an overview of applications of DDSMs. Part II focuses on the real DDSM, identifying what can go wrong and why. Part III presents state of the art solutions to problems that result from nonlinearities and finite states. The key issue addressed is spurious tones: how they arise and how to eliminate them. Part IV addresses complexity reduction strategies facilitated by error-masking.

Marketing Info

This tutorial is aimed at students, researchers, faculty, and practising engineers who are working with DSMs. Those who attend the tutorial will become familiar with the assumptions underlying conventional approaches to the design and operation of DDSMs, and the limitations thereof. They will be able to recognise nonideal behaviors that result from nonlinearity and finite states, and will be aware of state of the art solutions to optimize performance.

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Lecturer Bio

Michael Peter Kennedy is Professor of Microelectronic Engineering at University College Cork (UCC). He received the BE (Electronics) degree from UCD in 1984, the MS and PhD from the University of California at Berkeley in 1987 and 1991, respectively, and the DEng from the National University of Ireland in 2010. He joined UCC as Chair of the Department of Microelectronic Engineering in 2000. He served as Dean of the Faculty of Engineering from 2003 through 2005 and as Vice-President for Research from 2005 to 2011. He has over 320 research publications (including four patents) in the fields of oscillator design, hysteresis, neural networks, nonlinear dynamics, chaos communication, mixed-signal test, and frequency synthesis. He has worked as a consultant for SMEs and multinationals in the microelectronics industry and is founding Director of the Microelectronics Industry Design Association (MIDAS Ireland) and the Microelectronics Competence Centre of Ireland (MCCI).

He was made a Fellow of the Institute of Electrical and Electronic Engineers (IEEE) in 1998 for contributions to the theory of neural networks and nonlinear dynamics and for leadership in nonlinear circuits research and education. He has received many prestigious awards including Best Paper (International Journal of Circuit Theory and Applications), the 88th IEE Kelvin Lecture, IEEE Millenium and Golden Jubilee Medals, the inaugural Royal Irish Academy Parsons Award in Engineering Sciences, and the IEEE Solid-State Circuits Society Chapter of the Year Award 2010. In 2004, he was elected to membership of the Royal Irish Academy and was made a Fellow of the Institution of Engineers of Ireland by Presidential Invitation. From 2005 to 2007, he was President of the European Circuits Society and Vice-President of the IEEE Circuits and Systems (CAS) Society (with responsibility for Europe, Africa and the Middle East).

In 2012, he was appointed as a Distinguished Lecturer of the IEEE CAS Society and was elected Secretary for International Relations of the Royal Irish Academy.

Recent relevant publications:

1. Z. Ye and M.P. Kennedy. Reduced Complexity MASH Delta-Sigma Modulator. *IEEE Trans. Circuits and Systems-Part II*, 54(8):725-729, Aug. 2007.

2. K. Hosseini and M.P. Kennedy. Maximum Sequence Length MASH Digital Delta-Sigma Modulators. *IEEE Trans. Circuits and Systems-Part I*, 54(12):2628-2638, Dec. 2007 (MIDAS Ireland Outstanding PhD Research Publication 2008).

3. Z. Ye and M.P. Kennedy. Hardware Reduction in Digital Delta-Sigma Modulators via Error Masking — Part I: MASH DDSM. *IEEE Trans. Circuits and Systems-Part I*, 56(4):714-726, Apr. 2009.

4. Z. Ye and M.P. Kennedy. Hardware Reduction in Digital Delta-Sigma Modulators via Error Masking—Part II: SQ-DDSM. *IEEE Trans. Circuits and Systems-Part II*, 56(2):112-116, Feb. 2009.

5. K. Hosseini, M.P. Kennedy, S.H. Lewis and B.C. Levy. Prediction of the Spectrum of a Digital Delta-Sigma Modulator Followed by a Polynomial Nonlinearity. *IEEE Trans. Circuits and Systems-Part I*, 57(8):1905-1913, Aug. 2010.

6. K. Hosseini and M.P. Kennedy. *Minimizing Spurious Tones in Digital Delta-Sigma Modulators.* Springer, 2011. 148pp.

7. B. Fitzgibbon, M.P. Kennedy and F. Maloberti. Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part I: Constant Input. *IEEE Trans. Circuits and Systems-Part I*, 58(9):2137-2148, Sept. 2011.

8. B. Fitzgibbon, S. Pamarti and M.P. Kennedy. A Spur-Free MASH DDSM with High-Order Filtered Dither. *IEEE Trans. Circuits and Systems-Part II*, 58(9):585-588, Sept. 2011.

9. K. Hosseini, B. Fitzgibbon and M.P. Kennedy. Observations Concerning the Generation of Spurious Tones in Digital Delta-Sigma Modulators Followed by a Memoryless Nonlinearity. *IEEE Trans. Circuits and Systems-Part II*, 58(11):714-718, Nov. 2011.

10. M.P. Kennedy. Nested digital delta-sigma modulator, U.S. Provisional Appln. No. 61/576411, filed 16 December 2011.

11. M.P. Kennedy and B. Fitzgibbon. Pipelined Bus-Splitting Digital Delta-Sigma Modulator for Fractional-N Frequency Synthesizer System and Method, U.S. Provisional Appln. No. 61/653754, filed 31 May 2012.

12. B. Fitzgibbon, M.P. Kennedy and F. Maloberti. Hardware Reduction in Digital Delta-Sigma Modulators via Bus-Splitting and Error Masking—Part II: Non-constant Input. *IEEE Trans. Circuits and Systems-Part I*, **(*):***-***, ***. 2012 (in press).

13. M.P. Kennedy. Recent Advances in the Design, Analysis and Optimization of Digital Delta-Sigma Modulators. *Trans. IEICE,* **(*):***-***, ***. 2012 (in press).